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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Louis A. Lippincott Art Unit : 2623
Serial No.: 09/458,370 Examiner : R. Hesseltine
Filed : December 9, 1999 Assignee : Intel Corporation

Title : TWO-DIMENSIONAL INVERSE DISCRETE COSINE TRANSFORMING

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Commissioner for Patents
P.O. Box 1450
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BRIEF ON APPEAL

Applicant herewith files this Brief on Appeal, thereby perfecting the Notice of Appeal originally filed on August 30, 2004. The sections required by Rule 192 follow.

(1) Real Party in Interest

The application is assigned of record to Intel Corporation, who is hence the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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(3) Status of Claims

Claims 1, 4-8, 11-15, 19, 23, 25, and 28 are pending. Each of claims 1, 4-8, 11-15, 19, 23, 25, and 28 are under consideration and are hence appealed; and claims 2, 3, 9, 10, 16-18, 20-22, 24, 26 and 27 have been canceled.

(4) Status of Amendments

A request for reconsideration was filed on June 30, 2004. The request for reconsideration was indicated as having been considered.

(5) Summary of Claimed Subject Matter

The following provides a summary of claimed subject matter with illustrative citations in parentheses to (i) passages within the specification; and (ii) references contained in the accompanying drawings.

Claim 1 covers a method of implementing a two-dimensional inverse discrete cosine transform (see, inter alia, page 3, lines 2-5, Figs. 7 to 10). The method includes the step of executing first and second one-dimensional inverse discrete cosine transforming functions in first and second separate inverse discrete cosine transforming calculators (see, inter alia, page 7, lines 15-19). With this method, each of the first and second functions are controlled to operate on a matrix of coefficients with both of the first and second inverse discrete cosine transforming calculators operating simultaneously in a row direction at a first time and operating simultaneously in a column direction at a second time (see, inter alia, page 7, line 21 to page 8, line 1, Figs. 8 and 9).

Claim 4 includes the limitations of claim 1 and a sequencer which determines which direction each function operates in for a given matrix (see, inter alia, page 8, lines 15-18, Fig. 8).

Claim 6 includes the limitations of claim 1 and also provides that the functions are concurrently executed in the same direction on two different matrices of coefficients (see, inter alia, page 7, line 21 to page 8, line 1, Figs. 8 and 9).

Claim 7 includes the limitations of claim 1 and also provides that the functions are concurrently executed in the same direction and that the functions switch periodically and concurrently to the other direction (see, inter alia, page 7, line 21 to page 8, line 1, page 8, line 15 to page 9, line 12, Figs. 8 and 9).

Claim 8 covers a storage medium bearing a machine-readable program (57) (see, inter alia, page 9, lines 13-15, Figs. 7 to 10). The program is capable of causing a machine to execute two, one-dimensional inverse discrete cosine transforming functions in first and second inverse discrete cosine calculators (see, inter alia, page 7, lines 15-19). Each of the functions are controlled to operate on a matrix of coefficients with both of the first and second inverse discrete cosine calculators operating simultaneously in the row direction at a first time and in the column direction at a second time subsequent to the first time (see, inter alia, page 7, line 21 to page 8, line 1, Figs. 8 and 9).

Claim 11 includes the limitations of claim 8 and a sequencer that determines which direction each function operates in for a given matrix (see, inter alia, page 8, lines 15-18, Fig. 8).

Claim 13 includes the limitations of claim 8 and also provides that the functions are concurrently executed in the same direction on two different matrices of coefficients (see, inter alia, page 7, line 21 to page 8, line 1, Figs. 8 and 9).

Claim 14 includes the limitations of claim 8 and also provides that the functions are concurrently executed in the same direction, the functions switching periodically and concurrently to the other direction (see, inter alia, page 7, line 21 to page 8, line 1, page 8, line 15 to page 9, line 12, Figs. 8 and 9).

Claim 15 covers a method of implementing a two-dimensional inverse discrete cosine transform (see, inter alia, page 3, lines 2-5, Figs. 7 to 10). The method includes the steps of first executing a first one-dimensional inverse discrete cosine transforming function on a first inverse discrete cosine calculator, in a row direction on a first matrix of coefficients to produce a first matrix of intermediate results, second, after the first executing, on the first inverse discrete cosine calculator, executing a second one-dimensional inverse discrete cosine transform in a column direction on a second matrix of coefficients to produce another matrix of intermediate results, on a second inverse discrete cosine calculator, executing a third one-dimensional inverse discrete cosine transforming

function in the column direction on the first matrix of intermediate results concurrent with the second executing in the column direction on the second matrix of coefficients, and periodically switching the executing between the row and column directions (see, inter alia, page 7, line 15 to page 9, line 12, Figs. 8 and 9).

Claim 28, which is the last appended claim, but which is dependent on claim 15, includes the limitations of claim 15. It also provides that the second one-dimensional inverse discrete cosine transforming function and the third one-dimensional inverse discrete cosine transforming function occur concurrently in the same direction (see, inter alia, page 7, line 21 to page 8, line 1, Figs. 8 and 9).

Claim 19 covers a storage medium bearing a machine-readable program (57) (see, inter alia, page 9, lines 13-15, Figs. 7 to 10). The program is capable of causing a machine to execute a first one-dimensional inverse discrete cosine transforming function, where the first function executes in a row direction on a first matrix of coefficients, producing a matrix of intermediate results, execute a second one dimensional inverse discrete cosine transforming function in a column direction on a second matrix of coefficients, and execute a third one-dimensional inverse discrete cosine transforming function, where the second function executes in the column direction on the matrix of intermediate results concurrent with the execute a second function on the second matrix of coefficients (see, inter alia, page 7, line 15 to page 9, line 12, Figs. 7 to 10). With this program, the functions switch periodically and concurrently

between the row and column directions (see, inter alia, page 7, line 21 to page 8, line 1, page 8, line 15 to page 9, line 12, Figs. 8 and 9).

Claim 23 covers an apparatus implementing a two-dimensional inverse discrete cosine transform (see, inter alia, page 3, lines 2-5, Figs. 7 to 10). The apparatus comprises two one-dimensional inverse discrete cosine transform blocks (34, 36), a memory block (40), a sequencer block (38), and an address generator block (42). The sequencer block is alternately in a first state to control a column direction of operation of both one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation of both one-dimensional inverse discrete cosine transform blocks (see, inter alia, page 8, lines 15-18 and lines 21-23, Fig. 8). The address generator block generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (see, inter alia, page 8, lines 15-18).

Claim 25 covers a computer system including a processor (56) (see, inter alia, page 9, lines 13-20, Figs. 7 to 10). The system comprises first and second one-dimensional inverse discrete cosine transform blocks (34, 36), a memory block (40), a sequencer block (38), and an address generator block (42). The sequencer block alternates between a first state which controls both of the first and second one-dimensional inverse discrete cosine transform blocks to operate in a row direction, and a second state which controls both of the first and second one-dimensional inverse discrete cosine transform blocks to

operate in a column direction (see, inter alia, page 8, lines 15-18 and lines 21-23, Fig. 8). The sequencer block is alternately in one of two states, each state indicating the direction of operation of both one-dimensional inverse discrete cosine transform block (see, inter alia, Fig. 8). The address generator block generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (see, inter alia, page 8, lines 15-18).

(6) Grounds of Rejection

There is only one issue for review, and specifically, whether claims 1, 4-8, 11-15, 19, 23, 25, and 28 are properly rejected under 35 USC § 102 as being anticipated by US Pat. No. 5,268,853 to Tanaka ("Tanaka").

(7) Grouping of Claims

None of the claims rise and fall together except as specifically noted herein. Claim 5 rises and falls together with claim 1. Claim 12 rises and falls together with claim 8.

(8) Argument

To reiterate the above, claims 1, 4-8, 11-15, 19, 23, 25, and 28 stand rejected under 35 USC § 102, as allegedly being anticipated by Tanaka. This contention is respectfully traversed, and it is respectfully suggested that the rejection does not meet the Patent Office's burden of providing a prima facie showing of unpatentability.

The rejection contends that Tanaka describes an arrangement in which both of the inverse discrete coefficient (DCT) calculators operate in the same direction (i.e., column or row) at the same time. Tanaka, and specifically col. 11, lines 9-40 of Tanaka, does not disclose or suggest such an arrangement. Therefore, it is respectfully submitted that the rejection based on Tanaka does not meet the Patent Office's burden of providing a prima facie showing of unpatentability and that all pending claims are allowable.

Tanaka describes an arrangement in which different DCT calculators are used to read and write information (see, inter alia, Tanaka Fig. 5). Addresses are first designated in row direction such that calculated results provided by a first one-dimensional DCT calculator 4 are written to a memory device in the row direction (see, inter alia, Tanaka col. 11, lines 9-15, Fig. 10).

Thereafter, a switching circuit 18 of an address generator switches the row and column addresses designated in the memory device 2 (see, inter alia, Tanaka col. 11, lines 16-20). Next, data of a first address (0,0) is read and transmitted to a second one-dimensional DCT calculator 6 (see, inter alia, Tanaka col. 11, lines 20-22). Subsequently, the calculated results of the first one-dimensional DCT calculator 4 are written to the same address (0,0) as data (see, inter alia, Tanaka col. 11, lines 22-24). Next, the memory address is changed to (0,1) and the second one-dimensional DCT calculator 6 reads data of this address (see, inter alia, Tanaka col. 11, lines 24-26).

Thereafter, the calculated results of the first one-dimensional DCT calculator 4 are written to this address (0,1) as data (see, inter alia, Tanaka col. 11, lines 26-28).

After the reading and writing operations are performed at a last memory address, the row and column addresses in the memory are again switched and the process is repeated with the second one-dimensional DCT calculated reading data out of a memory address in the row direction and the calculated results of the first one-dimensional DCT calculator being written to the same address until a last memory address is reached (see, inter alia, Tanaka col. 11, lines 32-40).

Fig. 10 of Tanaka illustrates the operation of the two one-dimensional DCT calculators in which the arrow in the column direction shown by a solid line illustrates a first reading direction and the arrow in the column direction shown by a one-dotted chain line shows a second writing direction (see, inter alia, Tanaka col. 11, lines 28-32).

Tanaka's first one-dimensional DCT calculator executes a DCT formula in a row direction and the second one-dimensional DCT calculator executes a formula in the column direction (see, inter alia, Tanaka col. 7, lines 56-63, col. 8, lines 29-37). Tanaka also states that a switching circuit may cause the addresses in the memory device to switch to a row direction during a reading operation and thereafter switch to a column direction for a writing operation (see, inter alia, Tanaka col. 10, lines 20-24).

The rejection alleges, that Tanaka describes calculators operating simultaneously in the same direction (see, inter alia, Advisory Action of October 14, 2004, continuation of 5). However, there is no support for this position. It is respectfully submitted that Tanaka simply fails to disclose calculators simultaneously operating in the same direction.

Accordingly, as Tanaka fails to disclose the one-dimensional DCT calculators operating in the same direction at the same time, claims 1 and 5 should be allowable.

Claim 4 is independently allowable as Tanaka does not consider using a sequencer for determining the direction of operation for a function for a given matrix. Rather, Tanaka uses a switching circuit to switch, for example, a writing operation to occur in a column direction and a reading operation to occur in a row direction (see, inter alia, Tanaka col. 10, lines 27-31).

Claim 6 is also independently allowable as Tanaka does not describe the concurrent execution of the functions in the same direction on two different matrices of coefficients. Tanaka describes concurrent execution in two directions and describes operations relating to a single matrix of coefficients (e.g., the reading and writing operations pertaining to the memory device).

Claim 7 is also independently allowable as Tanaka fails to disclose both the concurrent execution of the two functions in

the same direction, as well as the periodic and concurrent switching between row and column directions.

Claims 8 and 12 are allowable for reasons similar to those proffered in connection with claims 1 and 5.

Claim 11 is independently allowable for reasons similar to those proffered in connection with claim 4.

Claim 13 is independently allowable for reasons similar to those proffered in connection with claim 6.

Claim 14 is independently allowable for reasons similar to those proffered in connection with claim 7.

Claim 15 and claim 28 dependent thereon, require the first and second inverse discrete cosine calculators to concurrently execute transforming functions in the column direction. These claims are also allowable because Tanaka, as noted above, does not disclose the concurrent execution of transforming functions in the same direction. Furthermore, claim 15 covers the concurrent and periodic switching of directions, a feature that is not disclosed in Tanaka.

Similar to claim 15, claim 19 also provides for concurrent and periodic switching of transforming functions, and as a result, this claims should be allowable.

Claim 23 includes a sequencer block that is alternately in a first state to control a column direction of operation of both

one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation of both one-dimensional inverse discrete cosine transform blocks. As both of the first and second states provide that the transform blocks are operating in the same direction (in both of the two operating states), these claims are not anticipated by Tanaka. In addition, Tanaka does not describe controlling the two transform blocks to cause them to operate in a single direction.

Claim 25 defines a sequencer block that alternates between a first state which controls both of the first and second one-dimensional inverse discrete cosine transform blocks to operate in a row direction, and a second state which controls both of said first and second one-dimensional inverse discrete cosine transform blocks to operate in a column direction. The sequencer block is alternately in one of two states, each state indicating the direction of operation of both one-dimensional inverse discrete cosine transform block. Tanaka does not disclose controllable states in which both transform blocks are operating in the same direction, and as such, claim 25 should be allowable.

In view of the above, it is again urged that none of the claims are unpatentable based on Tanaka. Reversal of the rejection, and a notice of allowance, is respectfully requested.

The brief fee of $950, including a two-month extension of time fee, is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Appendix of Claims

1. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing first and second one-dimensional inverse discrete cosine transforming functions in first and second separate inverse discrete cosine transforming calculators, each of the first and second functions being controlled to operate on a matrix of coefficients with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a row direction at a first time, and with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a column direction at a second time.

4. The method of claim 1 further comprising a sequencer which determines which direction each function operates in for a given matrix.

5. The method of claim 1 further comprising an address generator which generates an address for each coefficient in the matrix.

6. The method of claim 1 wherein the functions concurrently executed in the same direction on two different matrices of coefficients.

7. The method of claim 1 in which the functions are concurrently executed in the same direction, the functions switching periodically and concurrently to the other direction.

8. A storage medium bearing a machine-readable program capable of causing a machine to:

execute two, one-dimensional inverse discrete cosine transforming functions in first and second inverse discrete cosine calculators, each of the functions being controlled to operate on a matrix of coefficients with both of said first and second inverse discrete cosine calculators operating simultaneously in the row direction at a first time, and with both of said first and second inverse discrete cosine calculators operating simultaneously in the column direction at a second time subsequent to said first time.

11. The medium of claim 8 in which a sequencer determines which direction each function operates in for a given matrix.

12. The medium of claim 8 in which an address generator generates an address for each coefficient in the matrix.

13. The medium of claim 8 in which the functions are concurrently executed in the same direction on two different matrices of coefficients.

14. The medium of claim 8 in which the functions are concurrently executed in the same direction, the functions switching periodically and concurrently to the other direction.

15. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

first executing a first one-dimensional inverse discrete cosine transforming function on a first inverse discrete cosine calculator, in a row direction on a first matrix of coefficients to produce a first matrix of intermediate results;

second, after said first executing, on said first inverse discrete cosine calculator, executing a second one-dimensional inverse discrete cosine transform in a column direction on a second matrix of coefficients to produce another matrix of intermediate results;

on a second inverse discrete cosine calculator, executing a third one-dimensional inverse discrete cosine transforming function in said column direction on the first matrix of intermediate results concurrent with said second executing in the column direction on said second matrix of coefficients; and

periodically switching said executing between the row and column directions.

19. A storage medium bearing a machine-readable program capable of causing a machine to:

execute a first one-dimensional inverse discrete cosine transforming function, where the first function executes in a row direction on a first matrix of coefficients, producing a matrix of intermediate results;

execute a second one dimensional inverse discrete cosine transforming function in a column direction on a second matrix of coefficients;

execute a third one-dimensional inverse discrete cosine transforming function, where the second function executes in said column direction on the matrix of intermediate results concurrent with the execute a second function on the second matrix of coefficients,

in which the functions switch periodically and concurrently between the row and column directions.

23. An apparatus implementing a two-dimensional inverse discrete cosine transform, comprising:

two one-dimensional inverse discrete cosine transform blocks;

a memory block;

a sequencer block, the sequencer block alternately being in a first state to control a column direction of operation of both one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation of both one-dimensional inverse discrete cosine transform blocks; and

an address generator block which generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer.

25. A computer system including a processor, comprising:

first and second one-dimensional inverse discrete cosine transform blocks;

a memory block;

a sequencer block, which alternates between a first state which controls both of said first and second one-

dimensional inverse discrete cosine transform blocks to operate in a row direction, and a second state which controls both of said first and second one-dimensional inverse discrete cosine transform blocks to operate in a column direction, the sequencer block alternately being in one of two states, each state indicating the direction of operation of both one-dimensional inverse discrete cosine transform block; and

an address generator block which generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer.

28. A method as in claim 15, wherein said second one-dimensional inverse discrete cosine transforming function and said third one-dimensional inverse discrete cosine transforming function occur concurrently in the same direction.